In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 1, line 17 to page 2, line 7 as follows:

-- Figure 1 illustrates a pair of conventional synchronous FIFOs 101 and 102 connected to the expansion bus 100 of a conventional DSP. FIFO 101 permits the expansion bus to read in external data. FIFO 102 permits the expansion bus to write data out to external devices. The expansion bus 100 is normally only one of many peripheral interface devices connected to the direct memory access (DMA) within the DSP via a DMA control bus and a DMA data bus. The expansion bus clock XFCLK 103 is derived from DSP system clock and drives both the read clock of FIFO 101 and the write clock of FIFO 102. Data flows to the expansion bus port XD(N:0) 117 from FIFO 101 Q(N:0) output 105 via I/O path 104. Data flows to the D(N:0) input 106 of FIFO 102 from expansion bus port XD(N:0) 117 via I/O path 104. FIFO flags $\overline{PAE}$ 111 (almost empty flag) and $\overline{PAF}$ 112 (almost full flag) are two of the possible flags that may be used to signal respective interrupts INTy 110 and INTx 109 to the expansion bus interface 100. Another more simplified flag interface input from the active high half full flags HF 118 and 119 respectively to both the INTx 109 and INTy 110 expansion bus inputs is possible. Expansion bus enable signals 107 (XCEx, $\overline{XRE}$, $\overline{XOE}$ and $\overline{XOE}$) drive the enable logic 108 configured to control the FIFO enables as required. FIFO 101 inputs data on D(N:0) input 115 as timed by write clock 113. FIFO 102 output data on Q(N:0) output 116 as timed by read clock 114.--

Rewrite the paragraph at page 4, lines 3 to 13 as follows:

-- Consider the case of a digital signal processor with read bursts ~~trigger~~ triggered when the half full flag HF switches to an

active high state. When the HF flag switches from low to high, the digital signal processor initiates a read burst from the FIFO of length HF, which is half the FIFO depth. In digital signal processors without frame synchronization control, having synchronization events triggered from programmable FIFO flags such as HF is likely to produce problematical conditions. There are two separate problem conditions for a read burst. A similar analysis shows that the counterpart of these two scenarios can occur for write bursts to the FIFO.--

Rewrite the paragraph at page 11, lines 5 to 17 as follows:

-- Once the $\overline{ADV}$ pin 426 is set low (advanced mode), both $\overline{ADVPAF}$ 422 and $\overline{PAF}$ 412 go low at the same time 401, as $\overline{PAF}$ 412 would have gone low in the non-advanced mode (when $\overline{ADV}$=1). STARTFRM 415 is generated at 402. When $\overline{ADVPAF}$ 422 goes low at time 404 it triggers a DMA_Synch_Event 403 in the digital signal processor and the signal DMA_Frame 424 internal to the FIFO is asserted high at time 409. After the DMA Frame is completed as indicated by pulse 407 in ENDFRM 416, the $\overline{ADVPAF}$ pin 422 returns high at time 408 on the positive edge of the clock co-incident with the trailing edge of ENDFRM 416 at time 417. Note that during the DMA Frame interval 421 $\overline{PAF}$ 412 toggles once at times 405, 410, but there is no response in the $\overline{ADVPAF}$ signal 422 since the DMA_Frame 424 is still active during interval defined by 421.--

Rewrite the paragraph at page 11, lines 18 to 29 as follows:

-- The end of DMA_Frame signal 424 occurs at the rising edge of ENDFRM 416 at time 407. In one embodiment of the invention ENDFRM 416 is added as an additional FIFO pin that can receive a pulse from the digital signal processor signaling the end of the frame burst. In the alternate embodiment the generation of ENDFRM 416 is

handled by the FIFO (no ENDFRM pin) and the pulse 427 in ENDFRM 416 will be internal to the FIFO. This causes the DMA_Frame signal 424 in the FIFO to be de-asserted at time 419. After the completion of DMA_Frame signal 424, n-clocks 428 are appended to the DMA_Frame cycle during which time no new cycles may begin.--

Rewrite the paragraph at page 12, line 25 to page 13, line 5 as follows:

-- Figure 5 is an illustration of the DSP-FIFO interface similar to block diagram of Figure 1 as modified to incorporate the added signals ENDFRM 416 and $\overline{ADV}$ 426. These signals are needed to incorporate the functionality described to provide flexible control over the frame transfer operation. Statically setting the signal $\overline{ADV}$ 426 to an active low state changes the timing on the signal 511 to conform to the timing of $\overline{ADVPAF}$ 422. $\overline{ADVPAF}$ signal 511 supplies INTx input 509 of external bus 100. Similarly, for a digital signal processor performing write bursts to a FIFO 102 the identical signals ENDFRM 416 and $\overline{ADV}$ 426 allow the digital signal processor write FIFO 102 to generate an analogous signal $\overline{ADVPAE}$ 512 for write burst operation. $\overline{ADVPAE}$ signal 512 supplies INTy input 510 of external bus 100.--

Rewrite the paragraph at page 13, lines 6 to 24 as follows:

-- Figure 6 illustrates the status flag logic a portion of the FIFO block diagram (316 of Figure 3), showing the additional signals ENDFRM 416 and $\overline{ADV}$ 426 input to the status flag logic block 616. Four blocks internal to the status flag logic are illustrated. The frame size register 601 holds the value of the frame size programmed into the FIFO during the reset operation. When the FIFO operates from the programmed frame size value the frame size counter 602 is used to count words transferred during a

frame. The flag generation logic 603 keys off the completion cycle in the frame size counter 602 and the inputs from the flag input logic 604 to generate the flags $\overline{ADVPAF}$ ~~422~~ 425, $\overline{ADVPAE}$ 512, and ~~ADVHF~~ $\overline{ADVHF}$ 609. This option, the second embodiment of the invention allows for the digital signal processor to program the FIFO during the reset cycle passing the frame size and word count information to the FIFO via the offset registers 320. This allows the FIFO to generate on command the modified flag signals signal on its own without the otherwise required ENDFRM 416 and $\overline{ADV}$ 426 input signals.--